WT20-1809

Single LNB Supply and Control Voltage Regulator

Rev1.6 – 26 Jul. 2023

1. General description

Intended for analog and digital satellite receivers, this single low noise block converter regulator (LNBR) is a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to two LNB down converters via coaxial cables. The WT20-1809 requires few external components, with the boost switches and compensation circuitry integrated inside of the device. A high switching frequency is chosen to minimize the size of the passive filtering components, further assisting in cost reduction. The high level of component integration ensures extremely low noise and ripple figures. For DiSEqC™ communications, a tone control pin is provided to gate the internally-generated 22 kHz tone on-and-off.

A comprehensive set of fault registers are provided which, comply with all the common standards, including: overcurrent, thermal shutdown, under-voltage, and power not good.

The device uses a 2-wire bidirectional serial interface, compatible with the I²C™ standard, which operates up to 400 kHz.

A SLEEP pin is available to maximize power savings and to quickly shut down the device if needed, without I²C™ control.

The WT20-1809 is supplied in a lead (Pb) free package.

2. Features

- SLEEP pin for ultra-low power consumption mode
- Integrated boost MOSFET, current sensing, and compensation
- Stable with low-profile ceramic boost capacitors
- Adjustable LNB output current limit from 300 to 800mA
- Boost peak current limit scales with LNB current limit setting
- 8 programmable LNB output voltage (DAC) level
- LNB overcurrent limiter with shutdown timer
- Tracking boost converter minimizes power dissipation
- LNB transition times configurable by external capacitor
- Push-pull LNB output stage maintains 13.667→19.667V and 19.667→13.667V transition times, even with highly capacitive loads
- Built-in 22kHz tone oscillator facilitates DiSEqC™ tone encoding, even at no-load
- Tone generation does not require additional external components
- Diagnostic features : PNG, CPOK
- Extensive protection features : UVLO, OCP, TSD
- 2-wire serial I²C™-compatible interface

3. Applications

- Satellite Receivers
- Satellite-TV
- Satellite-PC

4. Package Information

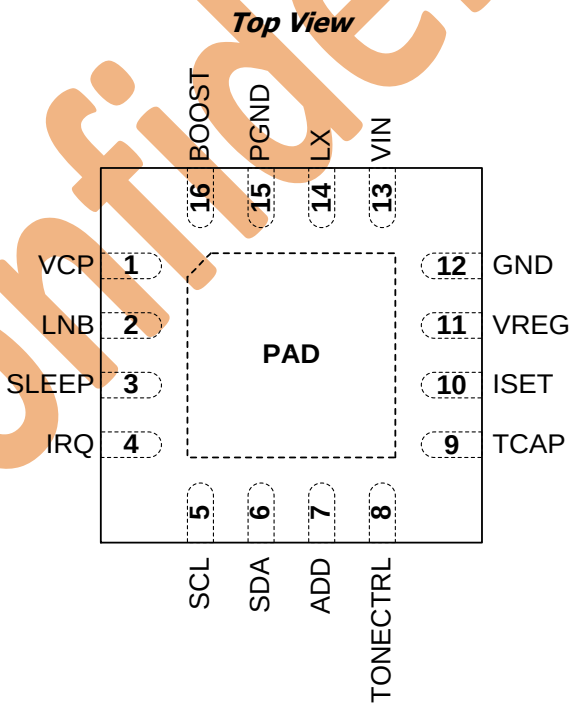
Type number	Package		
	Name	Description	Marking
WT20-1809	16QFN 3x3	QFN package(suffix ES)	WT1809

5. Package Thermal Characteristics

Package	$R_{\theta JA}$ (℃/W)	PCB
ES	47	4-Layer

6. Pin Information

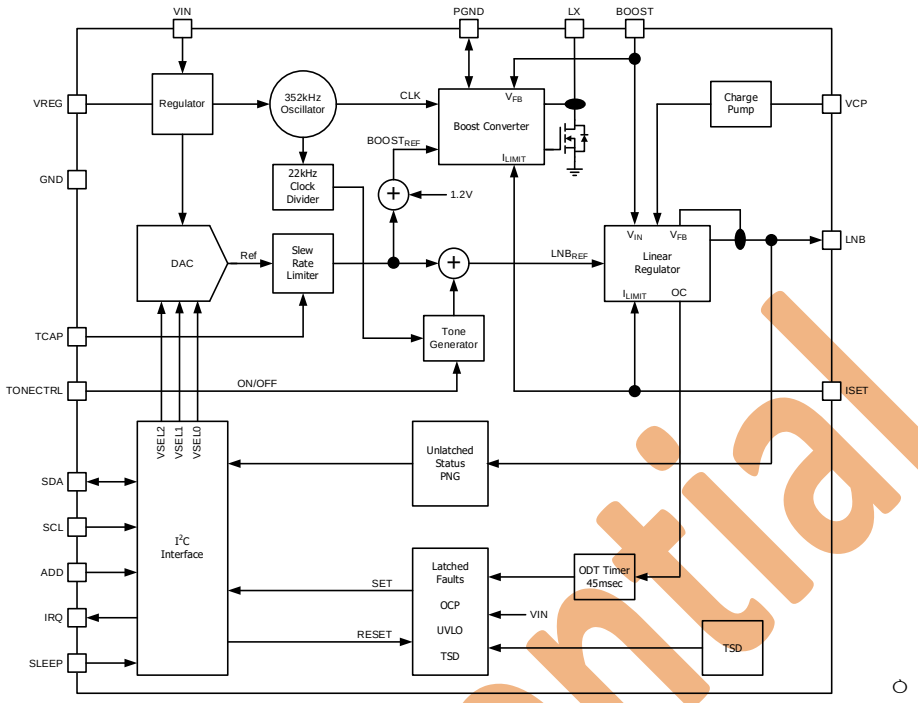
Top View



6. Pin Information (Continued)

Pin No.	Name	I/O	Function
1	VCP	O	Gate drive supply voltage and output of charge pump
2	LNB	O	Output voltage to LNB
3	SLEEP	I	Ultra-low power consumption mode input When this pin is pulled low, the WT20-1809 enters sleep mode; LNB output, boost and I²C™ communication disabled to reduce input quiescent current
4	IRQ	O	Interrupt request
5	SCL	I	I²C™-compatible clock input
6	SDA	I/O	I²C™-compatible data input/output
7	ADD	I	Address select
8	TONECTRL	I	Gates the 22kHz tone on-and-off
9	TCAP	I	Capacitor for setting the rise and fall time of the LNB output
10	ISET	I	Output current limit set via external resistor
11	VREG	O	Analog supply
12	GND	P	Signal ground
13	VIN	P	Supply input voltage
14	LX	O	Inductor drive point
15	PGND	P	Tracking supply voltage to linear regulator ground
16	BOOST	I	Tracking supply voltage to linear regulator

7. Block Diagram



8. Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact Wellang Sales Office/Distributors for availability and specifications.

Parameter	*Symbol*	*Value*	*Unit*
Load Supply Voltage, VIN pin	$V_{I(VIN)}$	30	V
Output Voltage; LNB and BOOST pins	$V_{O(LNB)}$,$V_{O(BOOST)}$	-0.3 ~ +40	V
Output Voltage; LX pin	$V_{O(LX)}$	-0.3 ~ +40	V
Output Voltage; VCP pin	$V_{O(VCP)}$	-0.3 ~ $V_{O(BOOST)}$ + 5.5	V
Logic Input Voltage	V_{LI}	-0.3 ~ +5.5	V
Logic Output Voltage	V_{LO}	-0.3 ~ +5.5	V
Maximum Junction Temperature	T_{JMAX}	+160	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Caution)

Values beyond absolute ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not guaranteed.

9. Recommended Operating Conditions

Over operating free-air temperature (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Input Operating Voltage	V_{IN}	10		16	V
Operating Ambient Temperature	T_A	-25		85	°C

10. Electrical Characteristics

T_A = 25°C, V_{IN}=12V, SLEEP pin = High or Open (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
General						
Output Voltage Accuracy	V_{OUT}	V_{IN} = 12V, I_{OUT} = 200mA, See table3 for DAC settings	-2	-	+2	%
Load Regulation	$\lvert\Delta V_{OUT(Load)}\rvert$	V_{IN} = 12V, V_{OUT} = 13.667V, ΔI_{OUT} = 50 to 200mA	-	35	70	mV
		V_{IN} = 12V, V_{OUT} = 19.000V, ΔI_{OUT} = 50 to 200mA	-	45	90	mV
Line Regulation	$\Delta V_{OUT(Line)}$	V_{IN} = 10 to 16V, V_{OUT} = 13.667V, I_{OUT} = 200mA	-10	0	10	mV
		V_{IN} = 10 to 16V, V_{OUT} = 19.000V, I_{OUT} = 200mA	-10	0	10	mV
Supply Current	$I_{IN(SLEEP)}$	SLEEP pin ≤ 0.8V, V_{IN} = 12V	-	80	220	µA
	$I_{IN(Off)}$	SLEEP pin ≥ 2.1V, EN bit = 0, V_{IN} = 12V	2.5	5	7.5	mA
	$I_{IN(On)}$[1]	EN bit = 1, V_{IN} = 12V, V_{BOOST}=20.2V, V_{OUT} = 19V, I_{LOAD} = 0mA, TONECTRL = 0	9	13	17	mA
		EN bit = 1, V_{IN} = 12V, V_{BOOST}=20.2V, V_{OUT} = 19V, I_{LOAD} = 0mA, TONECTRL = 1	11	15	21	mA
Boost Switch On Resistance[2]	$R_{DS(on)Boost}$	I_{SW} = 450mA	-	300	-	mΩ
Switching Frequency	f_{SW}		320	352	384	kHz
Linear Regulator Voltage Drop	ΔV_{REG}	V_{BOOST} – V_{LNB}, no tone signal, I_{LOAD} = 10mA	800	1200	1500	mV
TCAP Pin Current	I_{CHG}	TCAP capacitor charging	-15	-9.5	-6	µA
	I_{DISCHG}	TCAP capacitor discharging	6	9.5	15	µA

Notes)

1. In this mode, DC/DC converter is not being switched.
2. This item is guaranteed by design.

10. Electrical Characteristics (Continued)

T_A = 25°C, V_{IN}=12V, SLEEP pin = High or Open (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
General(Continued)						
Output Voltage Rise Time	$t_{r(VLNB)}$	For V_{LNB} 13.667 → 19.667V, C_{TCAP} = 100nF, I_{LOAD} = 0mA	-	9	-	ms
Output Voltage Pull-Down Time	$t_{f(VLNB)}$	For V_{LNB} 19.667 → 13.667V, C_{TCAP} = 100nF, I_{LOAD} = 0mA	-	10	-	ms
Output Sink Current	I_{RLNB}	EN bit = 0, VLNB =21V, Boost capacitor fully charged	4.5	8	11.5	mA
		EN bit = 1, VLNB =21V, TONECTRL = 0 or 1	13	18	26	mA
VREG Voltage	V_{VREG}	V_{IN} = 10V	4.5	5	5.5	V
ISET Voltage	V_{ISET}	V_{IN} = 10V	800	875	950	mV
TCAP Voltage	V_{TCAP}	V_{IN} = 10V, V_{OUT} = 13.667V	-	1.93	-	V
		V_{IN} = 10V, V_{OUT} = 19.000V	-	2.70	-	V
Protection Circuitry						
Output Overcurrent Limit	$I_{OUT(MAX)}$	R_{ISET} = 37.4kΩ	720	800	920	mA
Overcurrent Disable Time	t_{DIS}		40	45	50	ms
VIN Under-voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	8.0	8.35	8.7	V
VIN Turn On Threshold	$V_{IN(th)}$	V_{IN} rising	8.3	8.70	9.1	V
Under-voltage Hysteresis	$U_{VPLOHYS}$		-	350	-	mV

10. Electrical Characteristics (Continued)

T_A = 25°C, V_{IN}=12V, SLEEP pin = High or Open (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Protection Circuitry(Continued)						
Boost MOSFET Current Limit	$I_{BOOST(MAX)}$	R_{ISET} = 37.4kΩ	3.2	4.0	4.8	A
Thermal Shutdown Threshold	T_J		-	160	-	°C
Thermal Shutdown Hysteresis	ΔT_J		-	25	-	°C
Power Not Good Low	PNG_{LOSET}	With respect to V_{LNB} setting ; V_{LNB} low, PNG set to 1	88	91	94	%
	$PNG_{LORESET}$	With respect to V_{LNB} setting ; V_{LNB} low, PNG set to 0	92	95	98	%
Power Not Good Low Hysteresis	PNG_{LOHYS}	With respect to V_{LNB} setting	-	4	-	%
Power Not Good High	PNG_{HISET}	With respect to V_{LNB} setting ; V_{LNB} high, PNG set to 1	106	109	112	%
	$PNG_{HIRESET}$	With respect to V_{LNB} setting ; V_{LNB} high, PNG set to 0	102	105	108	%
Power Not Good High Hysteresis	PNG_{HIHYS}	With respect to V_{LNB} setting	-	4	-	%
Tone						
Amplitude	$V_{TONE(pp)}$	I_{LOAD} = 0 to 500mA, C_{LOAD} = 550nF	500	700	900	mV_{PP}
Frequency	f_{TONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 550nF	20	22	24	kHz
Duty Cycle	DC_{TONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 550nF	40	50	60	%
Rise Time(1)	t_{rTONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 550nF	5	10	15	µs
Fall Time(2)	t_{fTONE}	I_{LOAD} = 0 to 500mA, C_{LOAD} = 550nF	5	10	15	µs
Tone Control (TONECTRL Pin)						
Logic Input	$V_{TONECTRL(L)}$		-	-	0.8	V
	$V_{TONECTRL(H)}$		2.0	-	-	V
Sleep Mode Control (SLEEP Pin)						
Logic Input	$V_{SLEEP(L)}$		-	-	0.8	V
	$V_{SLEEP(H)}$		2.1	-	-	V
Input Pull-up Current			-35	-25	-19	µA

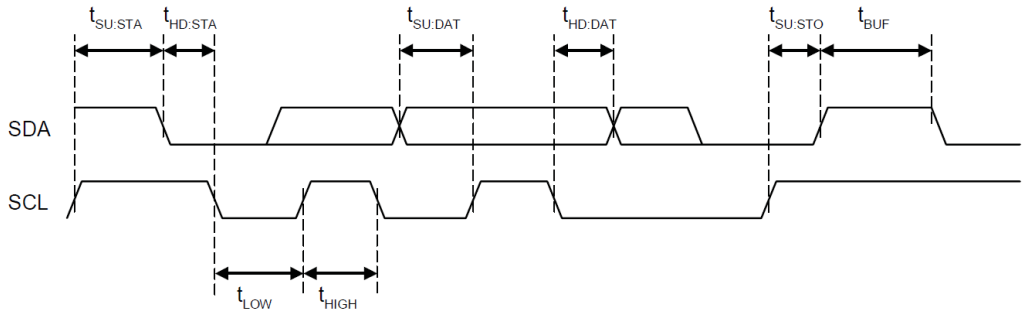
Notes)

1. Rise time (t_{rTONE}) is the time that it takes a signal to rise from 20% to 80% of the voltage between the low level and the high level.
2. Fall time (t_{fTONE}) is the time that it takes a signal to fall from 80% to 20% of the voltage between the low level and the high level.

10. Electrical Characteristics (Continued)

T_A = 25°C, V_{IN}=12V, SLEEP pin = High or Open (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I²C™-Compatible Interface						
Logic Input (SDA,SCL) Low Level	$V_{SCL(L)}$		-	-	0.8	V
Logic Input (SDA,SCL) High Level	$V_{SCL(H)}$		2.0	-	-	V
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 5V	-10	<±1	+10	μA
Logic Output Voltage SDA and IRQ	$V_{t2COut(L)}$	I_{LOAD} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{CLK}		-	-	400	kHz
Bus Free Time Between Stop/Start	t_{BUF}		1.3	-	-	μs
Hold Time Start Condition	$t_{HD:STA}$		0.6	-	-	μs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	-	-	μs
SCL Low Time	t_{LOW}		1.3	-	-	μs
SCL High Time	t_{HIGH}		0.6	-	-	μs
Data Setup Time	$t_{SU:DAT}$		100	-	-	ns
Data Hold Time	$t_{HD:DAT}$		0	-	900	ns
Rise Time of SDA and SCL signals	t_r		-		300	ns
Fall Time of SDA and SCL signals	t_f		-		300	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	-	-	μs
I²C™ Address Setting						
ADD Voltage for Address 0001,000	Address1		0	-	0.7	V
ADD Voltage for Address 0001,001	Address2		1.3	-	1.7	V
ADD Voltage for Address 0001,010	Address3		2.3	-	2.7	V
ADD Voltage for Address 0001,011	Address4		3.3	-	5.0	V



I²C™ Interface Timing Diagram

11. Functional Description

Protection

The WT20-1809 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

BOOST Converter/Linear Regulator

The WT20-1809 solution contains a tracking current-mode boost converter and linear regulator. The boost converter tracks the requested LNB voltage to within 1100 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOST}, is greater than the output voltage, V_{LNB}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the WT20-1809 is not exceeded.
The boost converter operates at 352 kHz typical: 16 times the internal 22 kHz tone frequency. All the loop compensation, current sensing, and slope compensation functions are provided internally.
The WT20-1809 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against short circuits. When the LNB output is shorted, the LNB output current is limited and the IC will be shut down if the overcurrent condition lasts for more than 45 ms. If this occurs, the WT20-1809 must be re-enabled for normal operation. The system should provide sufficient time between successive restarts to limit internal power dissipation; 1sec to 2sec is recommended.
In the case that two or more set top box LNB outputs are connected together by the customer (e.g., with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (e.g., 19V on the output of a 13V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the WT20-1809 output will auto-recover to their programmed levels.

Charge Pump
Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

LNB and BOOST Current Limits

The LNB output current limit, $I_{OUT(MAX)}$ can be by connecting a resister (R_{ISET}) from the ISET pin to GND as shown in the applications schematic. The LNB current limit can be set from 300 to 800mA, corresponding to an R_{ISET} value of 100 to 37.4 kΩ, respectively. If the LNB current limit is exceeded for more than the Overcurrent Disable Time (t_{DIS}) then the WT20-1809 will be shut down and the OCP bit set, as shown in figure 1. The WT20-1809 is guaranteed to support $I_{OUT} \leq 720$ mA continuously at 70 ℃ ambient with V_{IN} = 10 V and V_{OUT} = 20 V, The typical LNB output current limit can be set according to the following equation:

$$I_{OUT(MAX)} = 29.925 / R_{ISET},$$

where $I_{OUT(MAX)}$ is in mA and R_{ISET} is in kΩ. If the voltage at the ISET pin is 0 V (that is, shorted to GND), $I_{OUT(MAX)}$ will be clamped to a moderately high value(approximately 1.5 A). Care should be taken to ensure that ISET is not inadvertently grounded. If no resistor is connected to the ISET pin (that is, if ISET is open-circuit), $I_{OUT(MAX)}$ will be set to approximately 0 A and the WT20-1809 will not support any load (OCP will occur prematurely).

The BOOST pulse-by-pulse current limit, $I_{BOOST(MAX)}$, is automatically scaled along with the LNB output current limit. The typical BOOST current limit is set according to the following equation:

$$I_{BOOST(MAX)} = 4.7 \times I_{OUT(MAX)} + 270\ mA,$$

where both $I_{BOOST(MAX)}$ and $I_{OUT(MAX)}$ are in mA.

Automatically scaling the BOOST current limit allows the designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

Slew Rate Control

During either start-up, or when the output voltage at the LNB pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAP pin to GND (C_{TCAP} in the Applications Schematic). Note that during start-up, the BOOST pin is pre-charged to the input voltage minus a voltage drop. As a result, the slew rate control for the BOOST pin occurs from this voltage.

The value of C_{TCAP} can be calculated using the following formula:

$$C_{TCAP} = (I_{TCAP} \times 7) / SR,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAP} is the TCAP pin current specified in the datasheet. The recommended value for C_{TCAP}, 100 nF, should provide satisfactory operation for most applications.

The minimum value of C_{TCAP} is 10 nF. There is no theoretical maximum value of C_{TCAP}, however, too large a value will probably cause the voltage transition specifications to be exceeded. Tone generation is unaffected by the value of C_{TCAP}.

Pull-Down Rate Control

In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), the output linear stage provides approximately 45 mA of pull-down capability. This ensures that the output volts are ramped from 18V to 13V in a reasonable amount of time. When the tone is on (TONECTRL=1), the output linear stage must increase its pull-down capability to approximately 100 mA. This ensures that the signal meets all specifications, even with no load on the LNB output.

ODT (Overcurrent Disable Time)

If the LNB output current exceeds set output current, for more than 45 ms, then the LNB output will be disabled and the OCP bit will be set. See figure 1.

Short Circuit

If the LNB output is shorted to ground, the LNB output current will be clamped to $I_{OUT(MAX)}$. If the short circuit condition lasts for more than 45 ms, the WT20-1809 will be disabled and the OCP bit will be set.

In-Rush Current

At startup or during an LNB reconfiguration event, a transient surge current above the normal DC operating level can be provided by the WT20-1809. The current increase can be as high as the set output current, for as long as required, up to maximum of 45 ms.

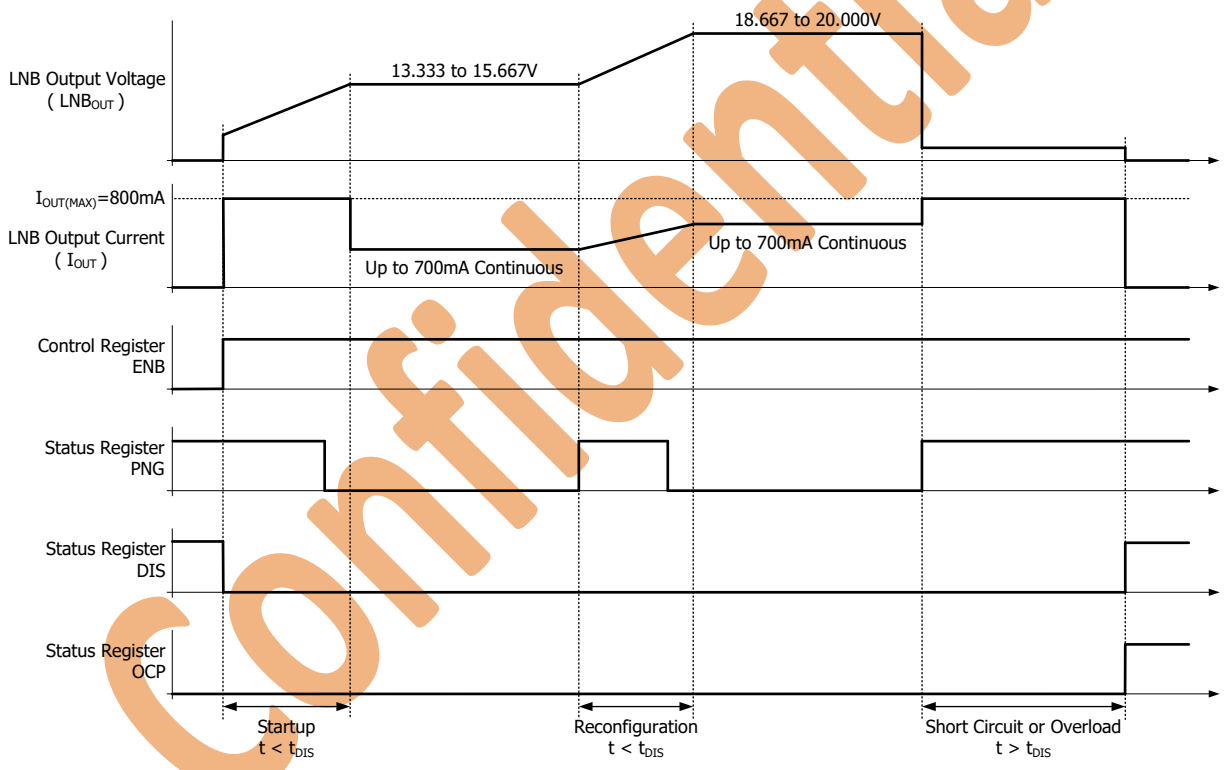


Figure 1. Startup, Reconfiguration and Short Circuit operation
Using $I_{OUT(MAX)}$ = 800 mA, R_{ISET} = 37.4 kΩ and a capacitive load

Tone Generation

A 22 kHz tone is generated internally, and can be controlled on and off via the TONECTRL pin as shown in figure 2. Note this tone can be generated under no-load conditions, and does not require the use of an external DiSEqC filter.

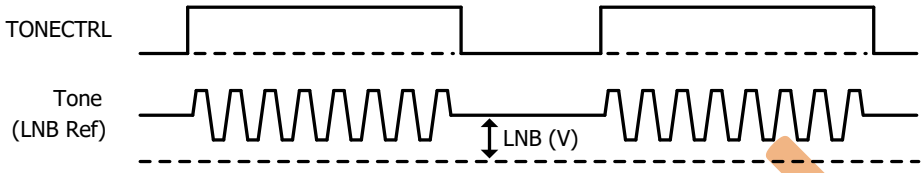


Figure 2. Internal tone, gated by TONECTRL pin

I²C™-Compatible Interface

The I²C™ interface is used to access the internal Control and Status register of the WT20-1809. This is a serial interface that uses two lines, serial clock (SCL) and serial data (SDA), connected to a positive supply voltage via a current source or a pull-up resistor. Data is exchanged between a microcontroller (master) and the WT20-1809 (slave). The master always generates the SCL signal. Either the master or the slave can generate the SDA signal. The SDA and SCL lines from the WT20-1809 are open-drain signals so multiple devices may be connected to the I²C™ bus. When the bus is free, both the SDA and the SCL lines are high.

SDA and SCL Signals
SDA can only be changed while SCL is low. SDA must be stable while SCL is high. However, an exception is made when the I²C™ Start or Stop condition is encountered. See the I²C™ Communication section for further details.

Acknowledge (AK) Bit
The Acknowledge (AK) bit indicates a "good transmission" and can be used to ways. First, if the slave has successfully received eight bits of either an address or control data, it will pull the SDA line low (AK=0) for the ninth SCL pulse to signal "good transmission" to the master. Second, if the master has successfully received eight bits of status data from the WT20-1809, it will pull the SDA line low for the ninth SCL pulse to signal "good transmission" to the slave. The receiver (either the master or the slave) should set the AK bit high (AK=1 or NAK) for the ninth SCL pulse if eight bits of data are not received successfully.

AK Bit During a Write Sequence
When the master sends control data (writes) to the WT20-1809 there are three instances where AK bits are toggled by WT20-1809. First, the WT20-1809 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W=0 for write). Second, the WT20-1809 uses the AK bit to indicate reception of a valid eight-bit Control register address. Third, the WT20-1809 uses the AK bit to indicate reception of eight bits of control data. This protocol is shown in Figure 3.

AK Bit During a Read Sequence
When the master reads status data from the WT20-1809 there are four instances where AK bits are sent three sent by the WT20-1809 and one sent by the master. First, the WT20-1809 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write (R/W=0 for write. Second, the WT20-1809 uses the AK bit to indicate reception of a valid eight-bit status register address. Third, the

WT20-1809 uses the AK bit to indicate reception of a valid seven-bit chip address plus a read/write (R/W=1 for read). Finally, the master uses the AK bit to indicate receiving eight bits of status data from the WT20-1809. This protocol is shown in Figure 4.

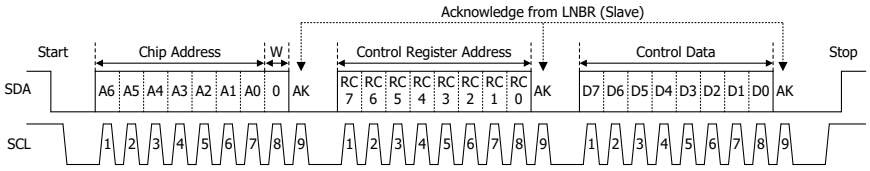


Figure 3. I²C Interface Write Sequences for Control Register

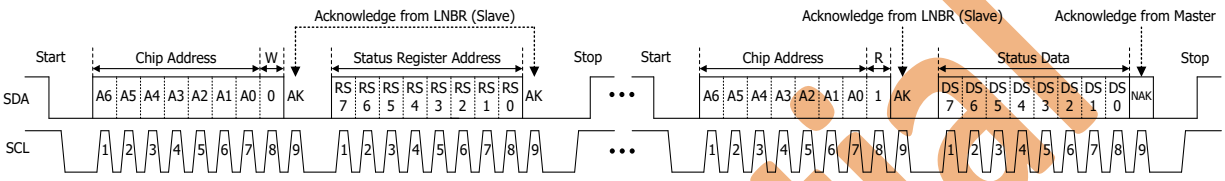


Figure 4. I²C Interface Reads Sequences for Status Register

I²C™ Communications

I²C™ Start and Stop Conditions

The I²C™ Start condition is defined by a negative edge on the SDA line while SCL is high. Conversely, the Stop condition is defined by a positive edge on the SDA line while SCL is high. The Start and Stop conditions are shown in Figure 3 and Figure 4. It is possible for the Start or Stop condition to occur at any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the WT20-1809 will respond by resetting the data transfer sequence.

I²C™ Write Cycle Description

Writing to the WT20-1809 Control register requires transmission of a total of 27 bits-three 8-bit bytes of data plus an Acknowledge bit after each byte. Writing to the WT20-1809 Control register is shown in Figure 3. Writing to the WT20-1809 Control register requires a chip address with R/W=0, a Control register address, and the control data, as follows;

- The Chip Address cycle consists of a total of nine bits-seven bits of chip address (A6 to A0) plus one read/write bit (R/W=0) to indicate a write from the master followed by an Acknowledge bit (AK=0 for reception of a valid chip address) from the slave. The chip address must be transmitted MSB (A6) first. The first five bits of the WT20-1809 chip address (A6 to A2) are fixed as 00010. The remaining two bits(A1 to A0) are used to select one of four possible WT20-1809 chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.
- The Control Register Address cycle consists of total of nine bit-eight bits of control register address (RC7 to RC0) from the master, followed by an Acknowledge bit from the slave. The Control register address must be transmitted MSB (RC7) first. The WT20-1809 only has one Control register, so the Control register address is fixed as 00000000.

- The Control Data cycle consists of a total of nine bits-eight bits of control data (D7 to D0) from the master followed by an Acknowledge bit form the slave. The control data must be transmitted MSB first (D7). The Control register bits are identified in the Control Registers section of this datasheet.

I²C™ Read Cycle Description

Reading from the WT20-1809 Status register requires transmission of a total of 36 bits-four 8 bit bytes of data plus an Acknowledge bit after each byte. Reading the WT20-1809 Status register requires a chip address with R/W=0, a Status register address, an I²C™ Stop condition, an I²C™ Start condition, a "repeated" chip address with R/W=1, and finally the status data form the WT20-1809. Reading from the WT20-1809 Status register is shown in Figure 4.

- This 9-bit Chip Address cycle is identical to the Chip Address cycle previously described for the Write Control register sequence. It consists of A6 to A0, plus one read/write bit (R/W=0) from the master, followed by an Acknowledge bit from the slave and finally an I²C™ Stop condition.
- The Status Register Address cycle consists of total of nine bit-eight bits of Status register address (RS7 to RS0) from the master, followed by an Acknowledge bit from the slave. The Status register address must be transmitted MSB (RS7) first. The WT20-1809 only has one Status register, so the Status register address is fixed as 00000000.
- The "Repeated" Chip Address cycle begins with an I²C™ Start condition followed by a 9-bit cycle identical to the Chip Address cycle previously described for the Write Control Register sequence. It consists of A6 to A0, plus one read/write bit (R/W=1) from the master, followed by an Acknowledge bit from the slave.
- The Status Data cycle consists of a total of nine bits-eight bits of control data (DS7 to DS0) from the master followed by an Acknowledge bit form the master. The Status data must be transmitted MSB first (DS7). The Status register bits are identified in the Status Registers section of this datasheet.

Interrupt Request (IRQ) and Fault Clearing

The WT20-1809 provides an interrupt request pin (IRQ), which is an open-drain, active-low output. This output may be connected to a common IRQ line with a suitable external pull-up and can be used with other I²C™-compatible devices to request attention from the master controller.

The IRQ output becomes active (active low) when the WT20-1809 recognizes a fault condition. The fault condition that will force IRQ active include under-voltage lockout (UVLO), overcurrent protection(OCP), and TSD faults are latched in the WT20-1809 Status register and will not be unlatched until the WT20-1809 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and Figure 5 for further details.

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read the status register of each to determine which device is requesting attention. As shown in Figure 5, the WT20-1809 latches all conditions in the Status register and sets in IRQ to logic low when a UVLO, OCP, or TSD event occurs. The IRQ bit is reset to logic high and the Status register is unlatched when the master acknowledges the status data form the WT20-1809 (an AK bit must be received form the master).

The disable (DIS) and Power Not Good (PNG) conditions do not cause an interrupt and are not latched in the Status register.

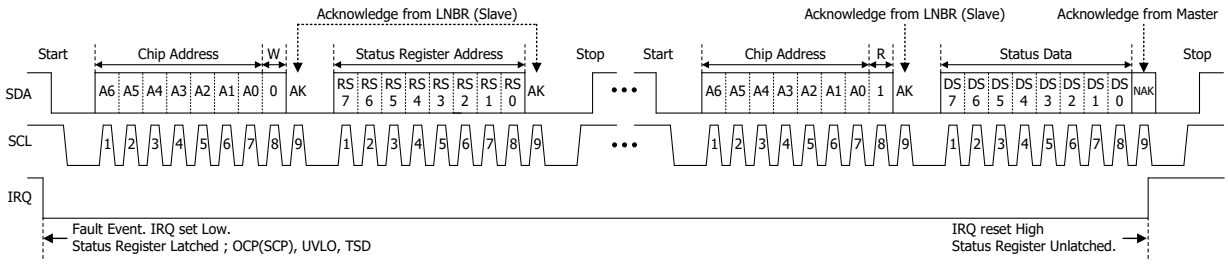


Figure 5. Fault, IRQ and Status Register Timing

Under-voltage Lockout (UVLO)

The WT20-1809 IRQ response to $V_{IN(UVLO)}$ is controlled by the I²C address setting. The WT20-1809 has two methods to control the IRQ for UVLO fault:

- The first method uses the I²C address setting (Address2, Address3 or Address4). In this method while V_{IN} is below 8.70 V (typ), the WT20-1809 is disabled and the I²C port is inactive. After V_{IN} rises above 8.70 V (typ), the I²C port becomes active and the IRQ pin is pulled low. An I²C Read cycle is required to report and clear the UVLO fault and set the IRQ pin to a logic high before the WT20-1809 can be enabled. If brown-out occurs, such that V_{IN} drops below 8.35 V (typ), the WT20-1809 will be disabled and the I²C port will become inactive (note that the IRQ pin will remain high during this time because the WT20-1809 is disabled). After V_{IN} rises above 8.70 V (typ) the I²C port reactivates and the IRQ pin is pulled low to report that a brown-out had occurred. An I²C Read cycle is required to report and clear the UVLO fault before the WT20-1809 can be re-enabled. A detailed timing diagram is shown in Figure 6.
- The second method uses I²C address setting (Address 1). In this method the I²C port is active when V_{IN} is above the I²C UVLO (6V when V_{IN} is rising). IRQ transitions low when V_{IN} goes above I²C UVLO (6V, V_{IN} rising), and the I²C Read cycle resets IRQ to logic high even if V_{IN} is below UVLO. Even though IRQ is cleared below UVLO, one more Read cycle is required after V_{IN} goes above UVLO, to re-enabled the WT20-1809. While V_{IN} is falling, IRQ transitions low when V_{IN} goes below UVLO, and the I²C Read cycle resets IRQ to logic high. A detailed timing diagram is shown in Figure 7.

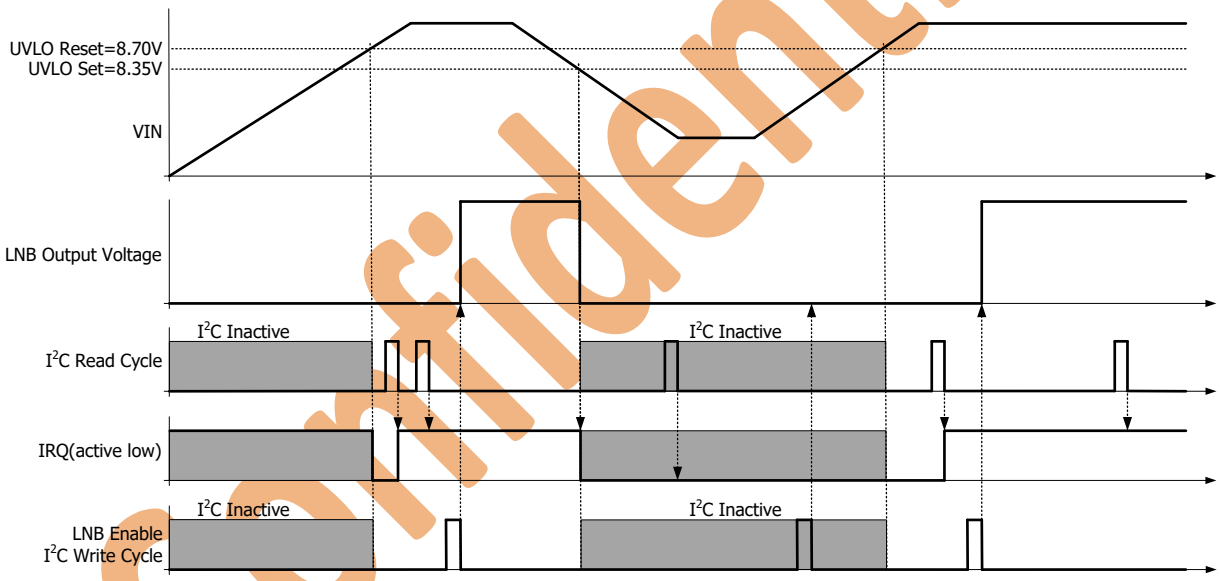


Figure 6. IRQ and Fault Sequence for I2C address set to address2, address3 and address4

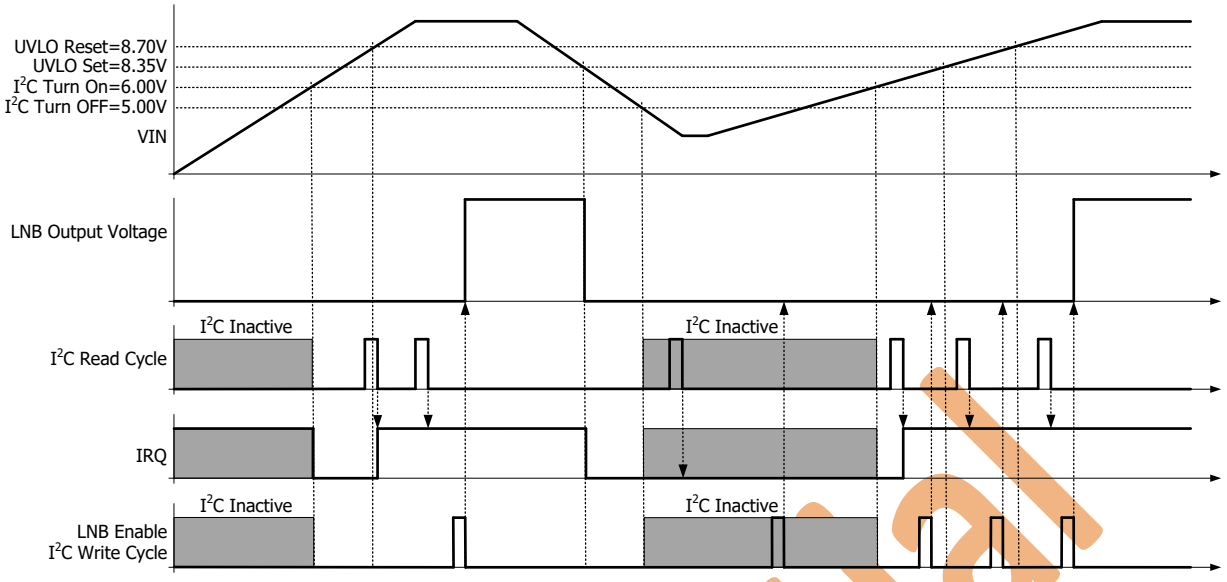


Figure 7. IRQ and Fault Sequence for I2C address set to address1

Overcurrent (OCP)

If the LNB output is grounded for more than 45 ms, the LNB output will be shut off, an overcurrent fault (OCP) will be latched in the Status Register, and the IRQ pin will transition low. After an OCP fault, the LNB does not respond to the Enable (ENB) bit until an I²C Read cycle is executed tor report and clear the OCP fault. After a successful I²C Read, the IRQ pin transitions high and the WT20-1809 can be re-enabled, provided the LNB output is no longer grounded. A detailed timing diagram is shown in Figure 8.

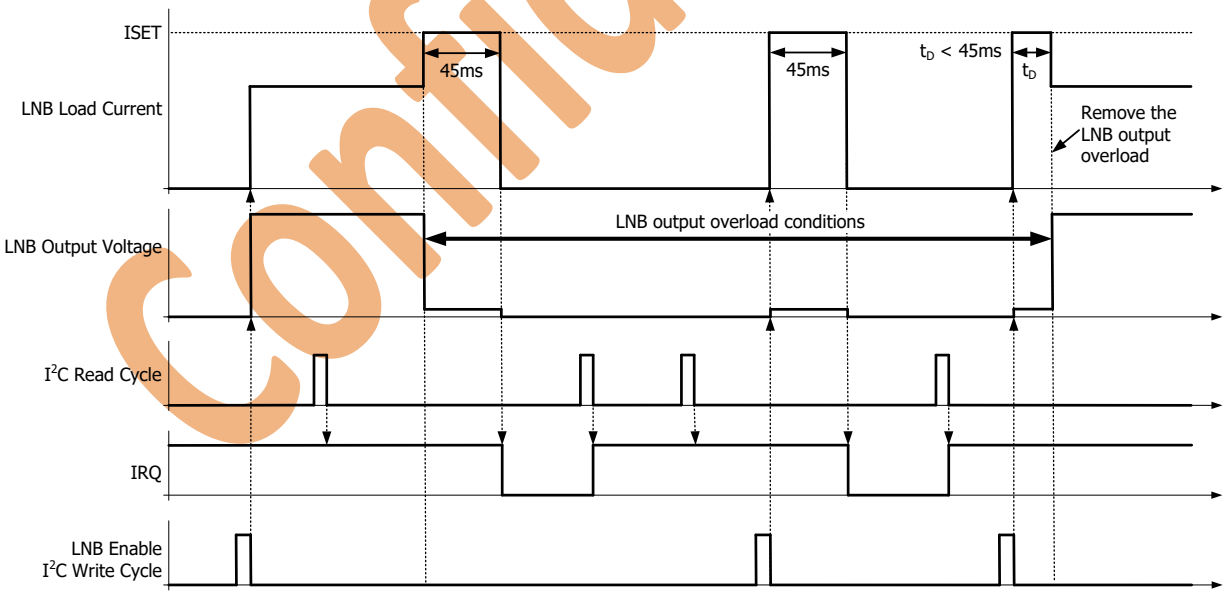


Figure 8. IRQ and Fault Sequence for Overcurrent (OCP)

Thermal Shutdown (TSD)

If the LNB junction temperature rises above 160℃ (typ), the LNB output will be shut off, a thermal shutdown fault (TSD) will be latched in the Status Register, and the IRQ pin will transition low. After a TSD fault the LNB output does not respond to the Enable (ENB) bit until and I²C Read cycle is executed to report and clear the TSD fault. After a successful I²C Read, the IRQ pin transitions high and the WT20-1809 can be re-enabled provided the junction temperature is below 135℃ (typ). A detailed timing diagram is shown in Figure 9.

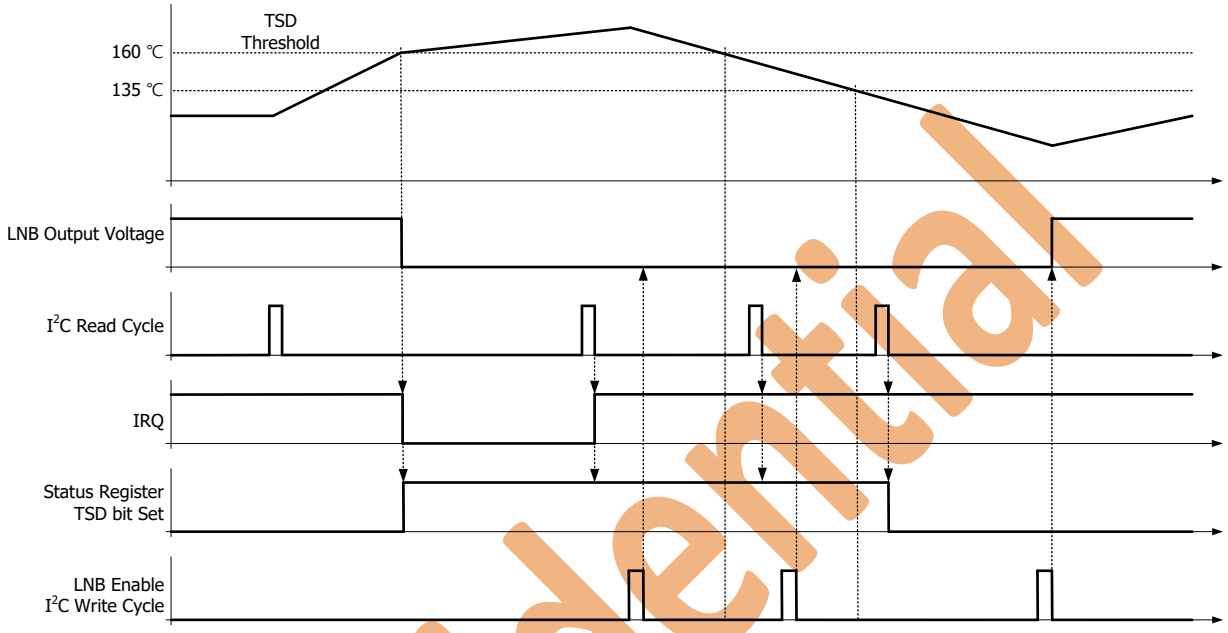


Figure 9. IRQ and Fault Sequence for Thermal Shutdown (TSD)

Control Registers (I²C™-Compatible Write Register)

All main functions of the WT20-1809 are controlled through the I²C™-compatible interface via the 8-bit Control registers. Table 2 shows the functionality and bit definitions of the Control register. At power-up, the Control register is initialized to all 0s.

Table 1. Control Register Bit Map

Bit	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Name	-	-	-	-	ENB	$VSEL_2$	$VSEL_1$	$VSEL_0$

Table 2. Control Register Description

Name	*Value*	*Meaning*	*Description*
$VSEL_0$		LNB output voltage control See Teable3 for available output voltage selections	The available voltages provide levels for all the common standards pulse the ability to add line compensation. VSEL0 is the LSB and VSEL2 is the MSB to the internal DAC.
$VSEL_1$			
$VSEL_2$			
ENB	0	Disable LNB Output	Turns the LNB output on or off.
	1	Enable LNB Output	
-			Not used
-			
-			
-			

Table 3. Output Voltage Amplitude Selection

$VSEL_2$	*$VSEL_1$*	*$VSEL_0$*	*LNB Output Voltage (V)*
0	0	0	13.333
0	0	1	13.667
0	1	0	14.333
0	1	1	15.667
1	0	0	18.667
1	0	1	19.000
1	1	0	19.667
1	1	1	20.000

Status Registers (I²C™-Compatible Read Register)

The main fault conditions: overcurrent (OCP) and thermal shutdown (TSD) are all indicated by setting the relevant bits in the Status registers. For these two fault cases, after the bit is set, it remains latched until the I²C™ master has successfully read the WT20-1809, assuming the fault has resolved.
The under-voltage lockout (UVLO) bit indicates either VIN is below VUVLO, or VREG is out of regulation. UVLO disables the LNB output and forces IRQ low. UVLO is a latched fault, and can only be cleared by performing an I²C™ READ cycle.

The Disable bit (DIS) indicates the status of the LNB output. The DIS is set when either a fault occurs (UVLO, OCP, TSD, or CPOK) or when the LNB output is turned off using the Enable bit (ENB) via the I²C™ interface. The DIS bit is latched and is only reset when there are no faults and the WT20-1809 output is turned back on using the Enable (ENB) bit via the I²C™ interface.

The Power Not Good (PNG) and Charge Pump OK (CPOK) bits are set based on the conditions sensed at the LNB output and VCP pins, respectively. These bits are not latched and, unlike the other fault bits, may become reset without an I²C read sequence. The PNG and CPOK bits are continuously updated.

There are three methods to detect when the Status register changes: responding to the interrupt request (IRQ) pin going low, continuously polling the Status register via the I²C interface, or detecting a fault condition external to the WT20-1809 and performing a diagnostic poll of the WT20-1809. In any case, the master should read and re-read the Status register until the status changes.

Table 4. Status Register Bit Setting

Bit	*Name*	*Function*	*Set*	*Reset Condition*	*Effect on IRQ*
0	DIS	LNB output disabled	Latched	LNB enabled and no faults	None
1	CPOK	Charge pump OK	Non-latched	$V_{CP} > V_{BOOST} + 1.5V$	None
2	OCP	Overcurrent	Latched	I²C read and $I_{LOAD} < I_{SET}$	IRQ set low
3	NA2	Not used	-	None	None
4	PNG	Power not good	Non-latched	LNB voltage within range	None
5	NA3	Not used	-	None	None
6	TSD	Thermal shutdown	Latched	I²C read and $T_J < 135℃$	IRQ set low
7	UVLO	VIN or VREG under-voltage	Latched	I²C read and $V_{IN} > 9.0V$	IRQ set low

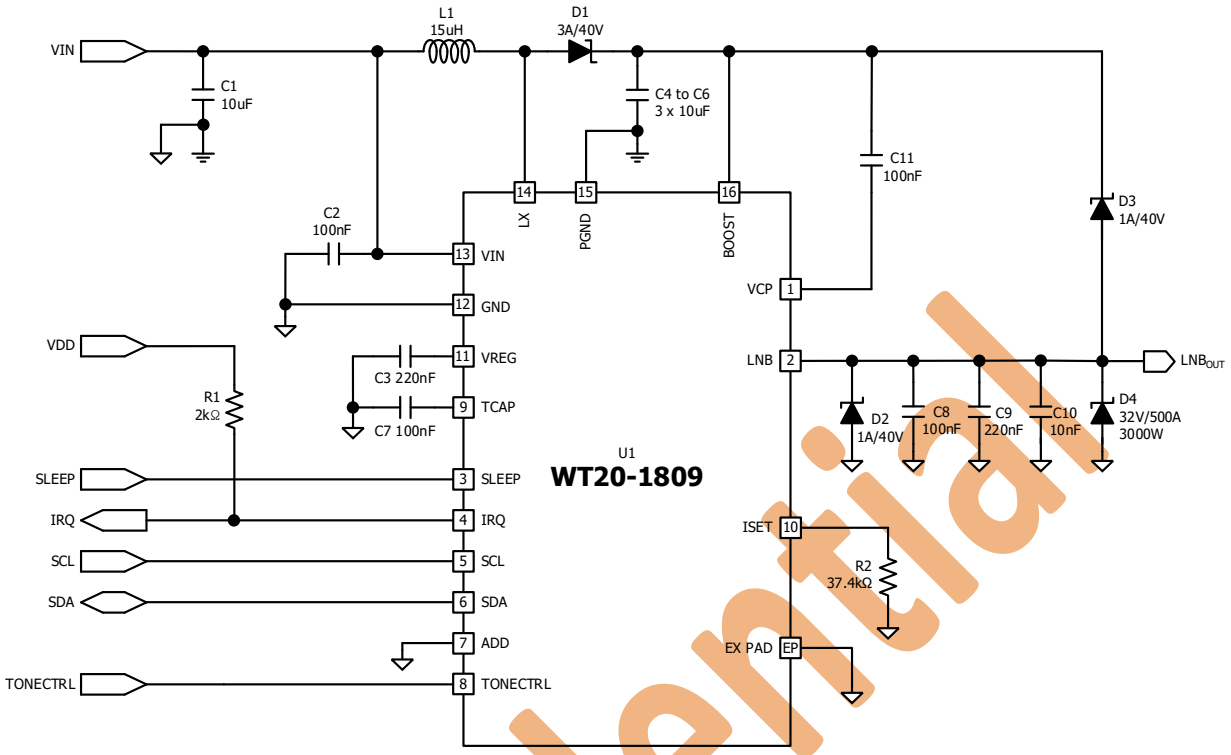
Table 5. Status Register Bit Map

Bit	7	6	5	4	3	2	1	0
Name	UVLO	TSD	NA3	PNG	NA2	OCP	CPOK	DIS

Table 6. Status Register Description

Name	Value	Meaning	Description
DIS	0	Normal Condition	The DIS bit is to 1 when the WT20-1809 is disabled, (ENB=0) or there is a fault condition ; UVLO, OCP, CPOK or TSD
	1	LNB disabled or Fault condition	
CPOK	0	VCP Not OK Condition	The CPOK bit is set 0 when the charge pump voltage is too low. If this bit is set 0, the LNB output is disabled and the DIS bit is set.
	1	Normal Condition	
OCP	0	Normal Operation	This bit will be set to a 1 if the LNB output current exceeds the overcurrent threshold ($I_{OUT(MAX)}$) for more than the overcurrent disable time (t_{DIS}). If the OCP bit is set to 1 then the DIS bit is also set to 1.
	1	Overcurrent Condition	
NA2	1	-	Not Used. This bit is always "1".
PNG	0	Normal Condition	Set to 1 when the WT20-1809 is enabled and the LNB output voltage is either too low or too high (nominally ±9% from the LNB DAC setting). Set to 0 when the WT20-1809 is enabled and the LNB voltage is within the acceptable range (nominally ±5% from the LNB DAC setting).
	1	Power Not Good Condition	
NA3	1	-	Not Used. This bit is always "1".
TSD	0	Normal Condition	The TSD bit is set to 1 if the WT20-1809 has detected an over-temperature condition. If the TSD bit is set to 1, then the DIS bit is also set to 1.
	1	Over-temperature Condition	
UVLO	0	Normal Condition	The UVLO bit is set to 1 if either the voltage at the VIN pin or the voltage at the VREG pin is too low. If the UVLO bit is set to 1, then the DIS bit is also set to 1.
	1	VIN under-voltage Condition	

12. Application Circuits



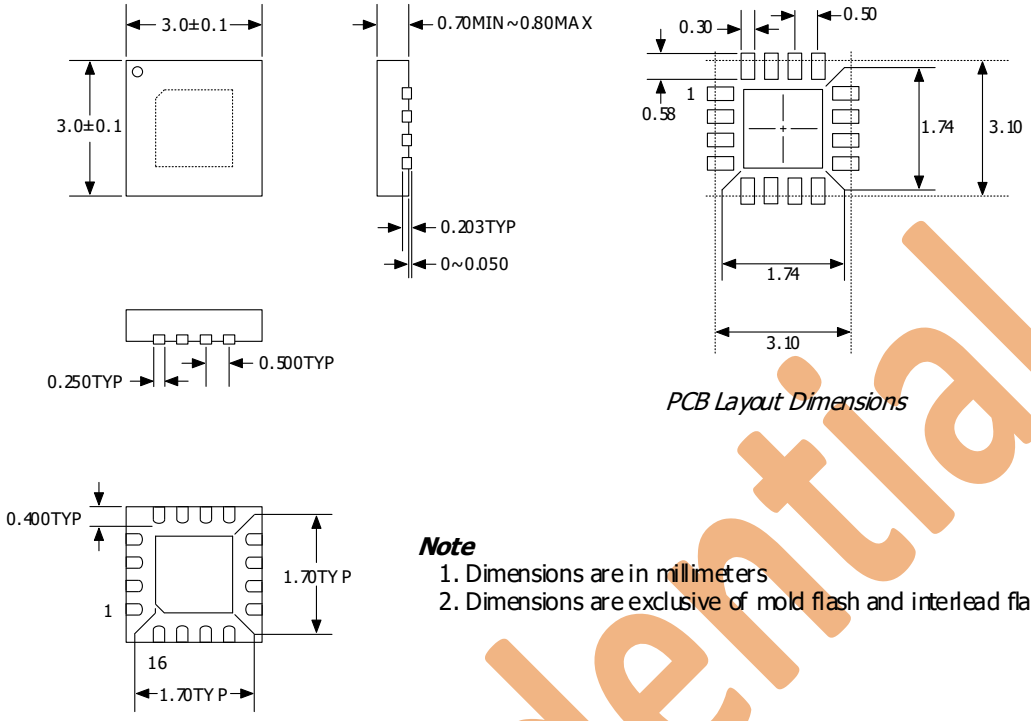
Schematic 1. WT20-1809 Typical Application

Table 7. Parts List

Part Reference	*Characteristics*	*Manufacture Device*	*Remark*
C2, C7, C8, C11	100nF/50V, X5R or X7R, 0603		
C3	220nF/10V_{MIN}, X5R or X7R, 0603		
C1, C4, C5, C6	3 x 10uF/35V, ±10%, X7R, 1210	Murata : GRM32ER7YA106K	
C9	220nF/50V, X5R or X7R, 0603		
C10	10nF/50V, X5R or X7R, 0603		
D1	Schottky Diode, 40V/3A, SMA	Sanken : SFPB-74 Vishay : B340A-E3/5AT Diodes, Inc : B340A-13-F	
D2, D3	Schottky Diode, 40V/1A, SMA	Diodes, Inc : B140HW-7 Central Senmi : CMMSH1-40	
D4	TVS Diode, 20VRM 32VCL at 500A (8/20us), 3000W SMC	Littelfuse : SMDJ20A ST : LNBTVS6-221S	
L1	15uH, ±10%, I_{SAT} > 3.1A DCR < 75mΩ	TDK : VLF10045T-150M3R5 Sumida : CDRH10D43FBNP-150M	
R1	2kΩ, 10%, 0402 or 0603		
R2	37.4kΩ, 1%, 0402 or 0603		

13. Package Outline

Package ES 16-Pin MLP/QFN



PCB Layout Dimensions

Note

1. Dimensions are in millimeters
2. Dimensions are exclusive of mold flash and interlead flash

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